

WHAT IS CLAIMED IS:

1. A thin film transistor matrix device comprising:
 - a transparent insulating substrate;
 - a plurality of thin film transistors arranged on the transparent insulating substrate in a matrix;
 - a plurality of picture element electrodes arranged on the transparent insulating substrate in a matrix and connected to the sources of the thin film transistors;
 - a plurality of bus lines for commonly connecting the gates or the drains of the thin film transistors;
 - outside terminals formed on a margin of the transparent insulating substrate and opposed to the ends of the bus lines; and
 - connection lines formed in regions inner of the outside terminals and commonly connecting said plurality of bus lines.
2. A thin film transistor matrix device according to claim 1, wherein
 - the connection lines include a plurality of connection lines, said plurality of gate bus lines which are adjacent to each other being respectively commonly connected to said plurality of connection lines.
3. A thin film transistor matrix device according to claim 2, further comprising
 - resistant lines which interconnect said plurality of connection lines and have a higher resistant value than the

connection lines.

4. A thin film transistor matrix device according to claims 1, wherein

said plurality of bus lines are electrically disconnected from the connection lines.

5. A thin film transistor matrix device comprising:
a transparent insulating substrate;

a plurality of thin film transistors arranged on the transparent insulating substrate in a matrix;

a plurality of picture element electrodes arranged on the transparent insulating substrate in a matrix and connected to the sources of the thin film transistors;

a plurality of gate bus lines for commonly connecting the gates of the thin film transistors;

a plurality of drain bus lines for commonly connecting the drains of the thin film transistors;

first outside terminals formed on a margin of the transparent insulating substrate and opposed to the ends of the gate bus lines;

second outside terminals formed on a margin of the transparent insulating substrate and opposed to the ends of the drain bus lines; and

gate connection lines formed in an inner region of the second outside terminals and commonly connecting said plurality of drain bus lines.

6. A thin film transistor matrix device according to

claim 5, further comprising

resistant lines for interconnecting the gate connection lines and the drain connection lines, and having a higher resistant value than the gate connection lines and the drain connection lines.

7. A thin film transistor matrix device according to claim 5, wherein

the gate connection lines include a first gate connection line and a second gate connection line, said plurality of gate bus lines which are adjacent to each other being respectively commonly connected to said first gate connection line and said second gate connection line;

the drain connection lines include a first drain connection line and a second drain connection line, said plurality of gate drain lines which are adjacent to each other being respectively commonly connected to said first drain connection and said drain connection line.

8. A thin film transistor matrix device according to claim 7, further comprising

resistant lines for interconnecting the first and the second gate connection lines, and the first and the second drain connection lines and having a resistant value than said plurality of connection lines.

9. A thin film transistor matrix device according to any one of claims 5 to 8, wherein

said plurality of gate bus lines are electrically

disconnected from the gate connection lines, and

said plurality of drain bus lines are electrically disconnected from the drain connection lines.

10. A liquid crystal panel comprising: a thin film transistor matrix device according to claim 1; an opposed substrate opposed to the thin film transistor matrix device; and a liquid crystal disposed between the thin film transistor matrix device and the opposed substrate.

11. A liquid crystal panel comprising: a thin film transistor matrix device according to claim 5; an opposed substrate opposed to the thin film transistor matrix device; and a liquid crystal disposed between the thin film transistor matrix device and the opposed substrate.

12. A liquid crystal unit comprising a liquid crystal panel according to claim 10; a circuit substrate having a circuit for driving the liquid crystal panel formed thereon; and connection lines for connecting the liquid crystal panel with the circuit substrate.

13. A liquid crystal unit comprising a liquid crystal panel according to claim 11; a circuit substrate having a circuit for driving the liquid crystal panel formed thereon; and connection lines for connecting the liquid crystal panel with the circuit substrate.

14. A method for fabricating a thin film transistor matrix device comprising:

a first step of forming on a transparent insulating

substrate a plurality of gate bus lines for commonly connecting the gates of thin film transistors, first outside terminals opposed to ends of the gate bus lines, and a gate connection line formed in a region inner of the first outside terminals for commonly connecting said plurality of gate bus lines;

a second step of forming a first insulating film on the entire surface; and

a third step of forming on the first insulating film a plurality of drain bus lines for commonly connecting the drains of the thin film transistors, second outside terminals opposed to the ends of the drain bus lines, and a drain connection line formed in a region inner of the second outside terminals for commonly connecting said plurality of drain bus lines.

15. A method for fabricating a thin film transistor matrix device comprising:

a first step of forming on a transparent insulating substrate a plurality of gate bus lines for commonly connecting the gates of thin film transistors, first outside terminals opposed to the ends of the gate bus lines, and a first gate connection line for commonly connecting the gate bus lines of one of groups in which adjacent ones of said plurality of gate bus lines are divided;

a second step of forming a first insulating film on

the entire surface;

a third step of forming on the first insulating film a plurality of drain bus lines for commonly connecting the drains of the thin film transistors, second outside terminals opposed to the ends of the drain bus lines, and a first drain connection line for commonly connecting the drain bus lines of one of groups in which adjacent ones of said plurality of drain bus lines are divided;

a fourth step of forming a second insulating film on the entire surface; and

a fifth step of forming on the second insulating film picture element electrodes, a second gate connection line for commonly connecting the gate bus lines of the other of the groups in which adjacent ones of said plurality of gate bus lines are divided, and a second drain connection line for commonly connecting the drain bus lines of the other of the groups in which adjacent ones of said plurality of drain bus lines are divided.

16. A method for fabricating a thin film transistor matrix device comprising:

a first step of forming on a transparent insulating substrate a plurality of gate bus lines for commonly connecting the gates of thin film transistors, first outside terminals opposed to the ends of the gate bus lines, a first gate connection line for commonly connecting the gate bus lines of one of groups in which adjacent ones

of said plurality of gate bus lines are divided, and a first drain connection line for commonly connecting the drain bus lines of one of groups in which adjacent ones of said plurality of drain bus lines are divided;

a second step of forming a first insulating film on the entire surface; and

a third step forming on the first insulating film said plurality of drain bus lines for commonly connecting the drains of the thin film transistors, second outside terminals opposed to the ends of the drain bus lines; a second drain connection line for commonly connecting the drain bus lines of the other of the groups in which adjacent ones of said plurality of drain bus lines are divided, and a second gate connection line for commonly connecting the gate bus lines of the other of the groups in which adjacent ones of said plurality of gate bus lines are divided.

17. A method for fabricating a thin film transistor matrix device comprising:

a first step of forming on a transparent insulating substrate a plurality of gate bus lines for commonly connecting the gates of thin film transistors, first outside terminals opposed to the ends of the gate bus lines, a first gate connection line for commonly connecting the gate bus lines of one of groups in which adjacent ones of said plurality of gate bus lines are divided, and a

first drain connection line for commonly connecting the drain bus lines of one of groups in which adjacent ones of said plurality of drain bus lines are divided;

a second step of forming a first insulating film on the entire surface;

a third step of forming on the first insulating film said plurality of drain bus lines for commonly connecting the drains of the thin film transistors, second outside terminals opposed to the ends of the drain bus lines, a second drain connection line, and a second gate connection line;

a fourth step of forming a second insulating film on the entire surface; and

a fifth step of forming on the second insulating film picture element electrodes, a first connection line for connecting the drain bus lines of the other of the groups in which adjacent ones of said plurality of drain lines are divided to the second drain connection line, and a second connection line for connecting the gate bus lines of the other of the groups in which adjacent ones of said plurality of gate bus lines are divided to the second gate connection line.

18. A method for fabricating a thin film transistor matrix device according to claim 14, further comprising

a fourth step of forming a second insulating film on the entire surface after the third step; and

a fifth step of forming on the second insulating film picture element electrodes, and a resistant line for interconnecting the gate connection lines and the drain connection lines.

19. A method for fabricating a thin film transistor matrix device according to claim 16, further comprising

a fourth step of forming a second insulating film on the entire surface after the third step; and

a fifth step of forming on the second insulating film picture element electrodes, and a resistant line for interconnecting the gate connection lines and the drain connection lines.

20. A method for fabricating a thin film transistor matrix device according to claim 15, wherein

in the fifth step resistant lines for interconnecting the first and the second gate connection lines and the first and the second drain connection lines are formed.

21. A method for fabricating a thin film transistor matrix device according to claim 17, wherein

in the fifth step resistant lines for interconnecting the first and the second gate connection lines and the first and the second drain connection lines are formed.

22. A method for fabricating a thin film transistor matrix device according to claim 14, wherein

after the fabrication steps are over, the gate bus lines are electrically disconnected from the gate

connection lines, and the drain bus lines are electrically disconnected from the drain connection lines.